

Agilent Technologies *PCI Express® (PCIe®)*



*Test Solution Overview Using
the Agilent E5071C ENA
Option TDR*

Last update: 2013/04/24 (HK)

Purpose

- This slide will show how to make measurements of PCI Express® Compliance Testing by using the Agilent E5071C ENA Option TDR.

Agilent Digital Standards Program

Our solutions are driven and supported by Agilent experts involved in international standards committees:

- Joint Electronic Devices Engineering Council (JEDEC)
- **PCI Special Interest Group (PCI-SIG®)**
- Video Electronics Standards Association (VESA)
- Serial ATA International Organization (SATA-IO)
- USB-Implementers Forum (USB-IF)
- Mobile Industry Processor Interface (MIPI) Alliance
- Optical Internetworking Forum (OIF)

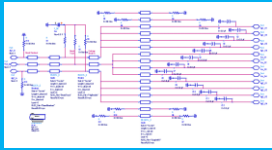
We're active in standards meetings, workshops, plugfests, and seminars

Our customers test with highest confidence and achieve compliance faster

The JEDEC logo consists of the word "JEDEC" in a bold, blue, sans-serif font.The PCI EXPRESS logo features the text "PCI EXPRESS" in a bold, black, sans-serif font, with a blue arrow graphic pointing to the right.The SERIAL ATA logo includes the text "SERIAL ATA" in a bold, blue, sans-serif font, with a yellow and blue graphic element.The D logo is a large, bold, black letter "D" with a white outline.The HDMI logo features the text "HDMI" in a bold, black, sans-serif font, with "HIGH-DEFINITION MULTIMEDIA INTERFACE" in a smaller font below it.The USB logo includes the text "USB" in a bold, blue, sans-serif font, with a red and white graphic element.The MIPI logo features the text "mipi" in a lowercase, blue, sans-serif font, with "mobile industry processor interface" in a smaller font below it.The OIF logo includes the text "OIF" in a bold, blue, sans-serif font, with "OPTICAL INTERNETWORKING FORUM" in a smaller font below it.

PCIe – Agilent Total Solution

Physical layer – interconnect design



ADS design software



86100D DCA-J/TDR



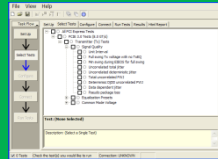
E5071C ENA option TDR

Industry's lowest scope noise floor/sensitivity and trigger jitter

Physical layer-transmitter test



90000 X-Series oscilloscope



N5393C PCI Express electrical compliance software



86100CU-400 PLL and Jitter Spectrum Measurement SW

DSA-X Series & Q Series

Physical layer-receiver test



J-BERT N4903B –complete receiver tolerance



N4916B 4-tap de-emphasis signal converter



N4880A Clock Multiplier



N5990A automated compliance and device characterization test software

Automated compliance software – accurate, efficient and consistent

Data link/transaction layer



• U4301A Protocol Analyzer

- U4305A Exerciser
- Protocol Test Card

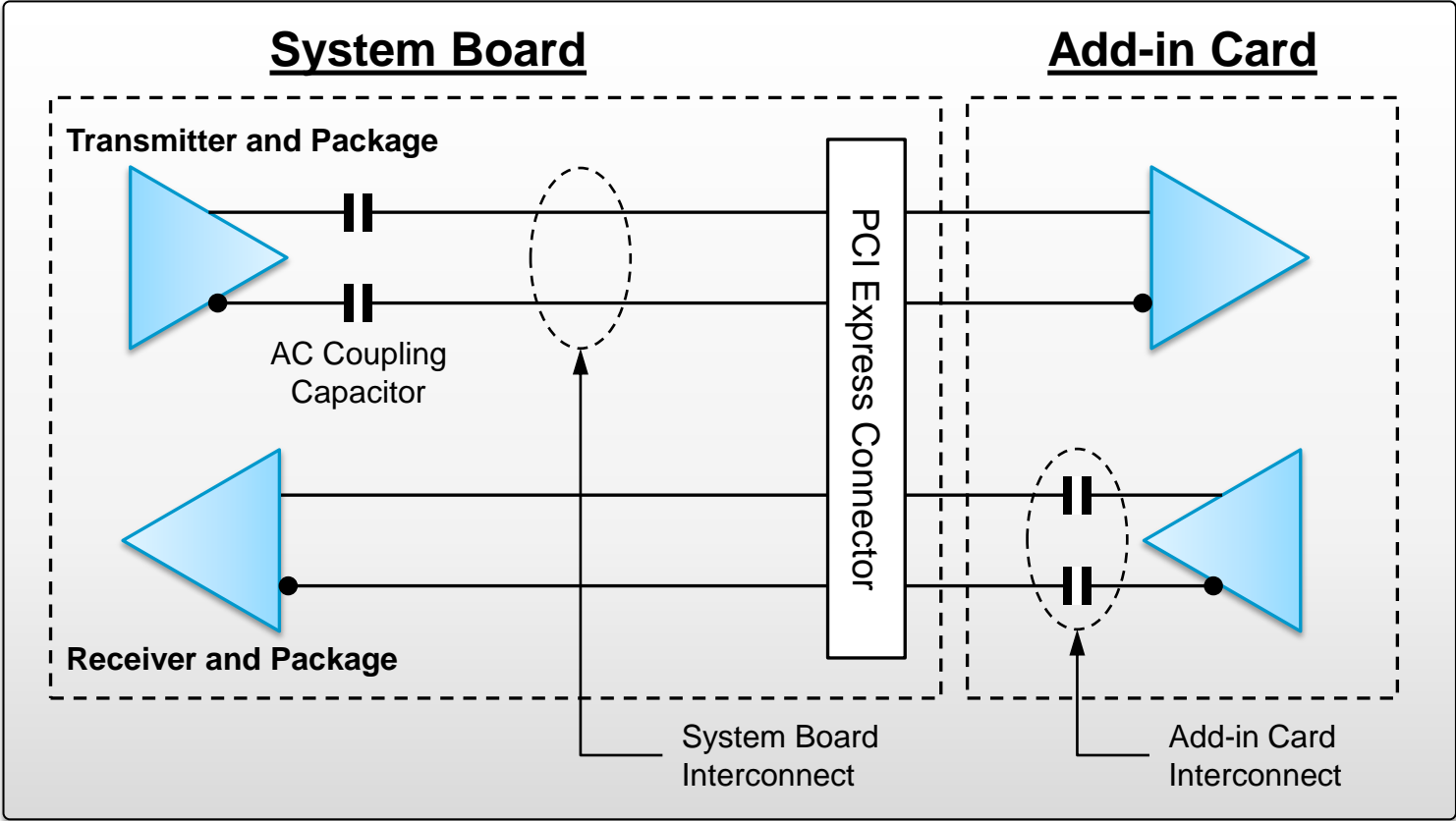
- Multiple probes with ESP technology



X1 through x16 Analysis and Exerciser support, with industry's only ESP probing technology



PCIe PHY Electrical Architecture



Full-duplex for each lane (Tx and Rx)

PCIe 3.0 Specs and Compliance Program Overview

with PHY Electrical Test Items

Spec.

BASE Specification Revision 3.0
Card Electromechanical (CEM) Specification Revision 3.0

- Tx/Rx Return Loss Test @BASE Spec.
- PCB Impedance Test @CEM Spec.

CTS

Architecture PHY Test Specification Revision 3.0

- PCB Impedance Test

Workshop

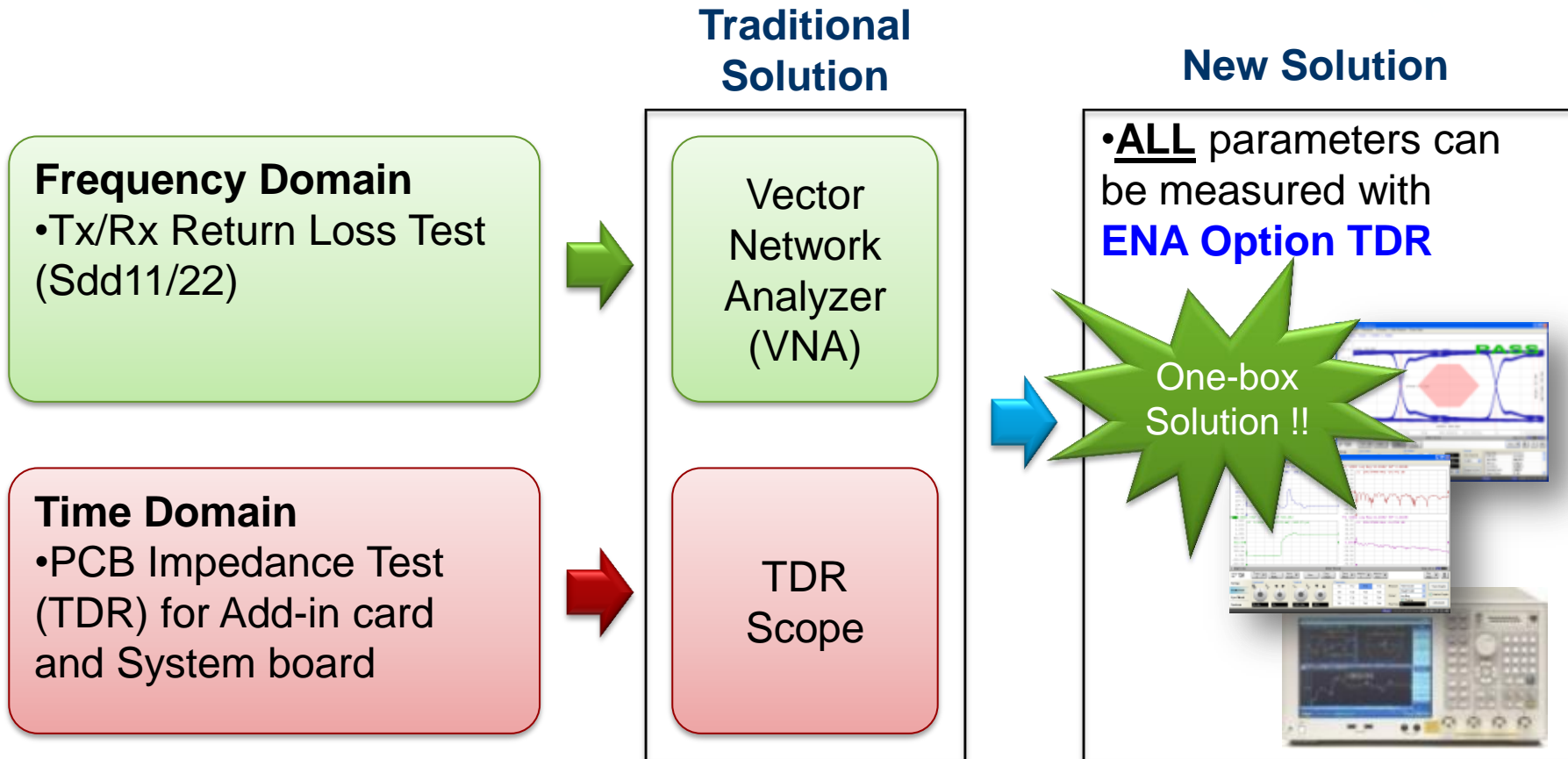
Gold Suites (Compliance Program)

[Integrators List](#)

PCIe 3.0 Test Solution

Solution Overview using E5071C ENA Option TDR

- PCIe 3.0 compliance testing requires parametric measurements in both time and frequency domains



PCIe 3.0 PCB Impedance Test Solution

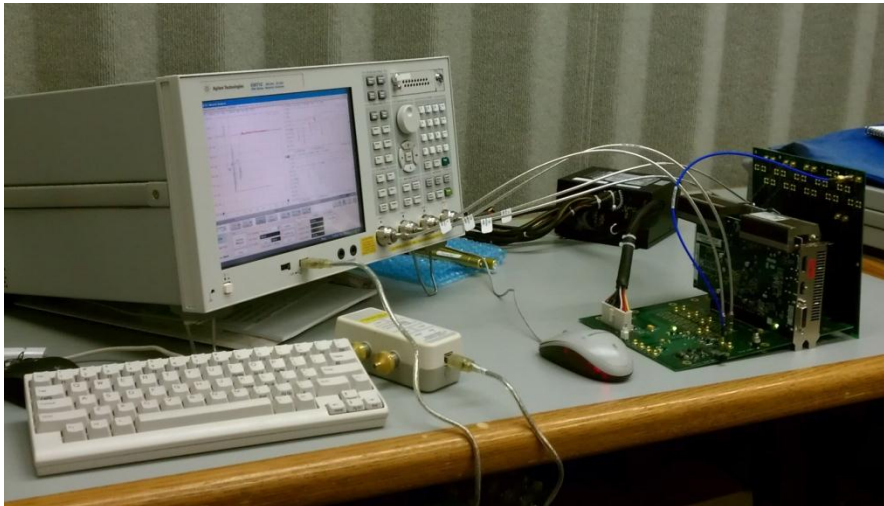
Measurement Parameters

◆ PCB Impedance Test

	2.5 GT/s	5 GT/s	8 GT/s
Differential Impedance	N/A	68 - 105 Ω	70 - 100 Ω

This applies to both the add-in card and the system board.

Measurement example of Add-in card PCB trace impedance test:



PCIe 3.0 PCB Impedance Test Solution

ENA Option TDR Solution



- ENA Mainframe
 - E5071C-4K5: 4-port, 300kHz to 20GHz
- Enhanced Time Domain Analysis Option (E5071C-TDR)
- ECal Module
 - N4433A for E5071C-4K5

- Method of Implementation (MOI) document available for download on Agilent.com, and state files will be available soon.

PCI Express 3.0 ENA Differential Impedance Test Procedures for Add-in Cards & Motherboard (system) Testing using Agilent E5071C ENA Network Analyzer with Option TDR

MOI

Version 0.8
October 16, 2012

(Method of Implementation)

Step-by-step procedure on how to measure the specified parameters in the specification document using ENA Option TDR.

www.agilent.com/find/ena-tdr_compliance

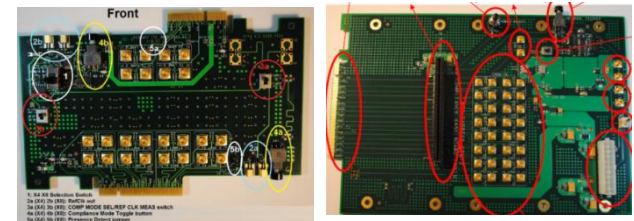
www.agilent.com/find/ena-tdr_pcie-pcb

PCI Express Test Fixtures

Specialized test fixtures available from the PCI-SIG:

- The **Compliance Load Board (CLB)** is used for testing platforms.
- The **Compliance Base Board (CBB)** is used for testing add-in cards.

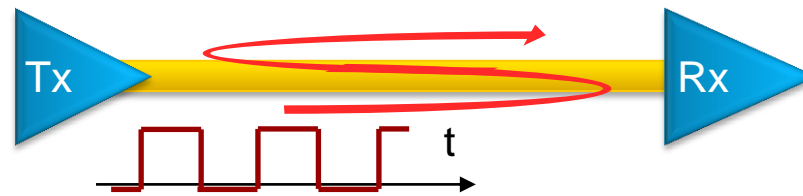
The following links provide copies of the draft [CLB 3.0 Test Fixture User's Document](#) and the [CBB 3.0 Test Fixture User's Document](#). [Go to the CLB and CBB ordering instructions for more information.](#)



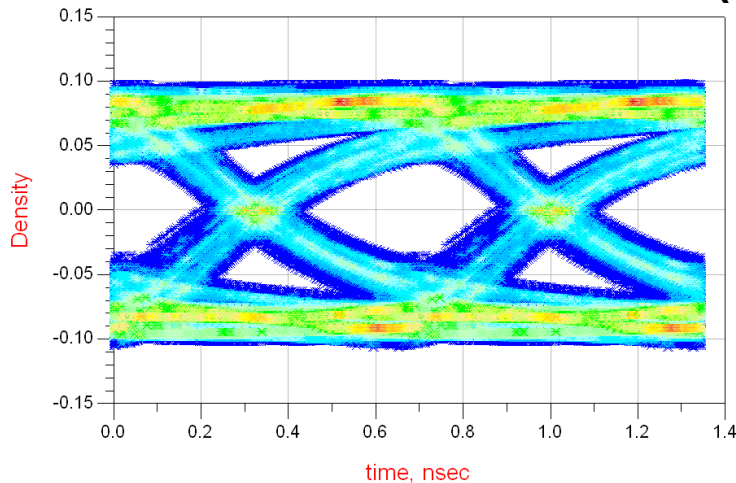
Importance of Tx/Rx Interface Characterization

◆ Why measure S-parameter and impedance on Tx/Rx device?

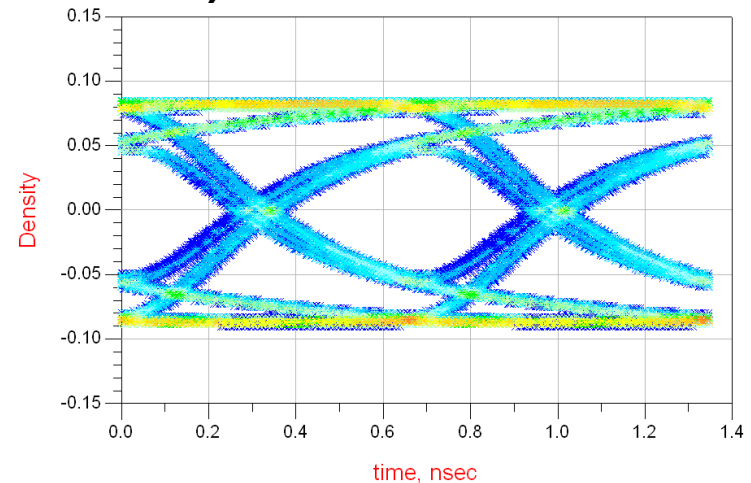
A portion of the transmitted signal is reflected from the receiver due to impedance mismatches. If the transmitter is not impedance matched, additional reflections occur, causing eye closure. For high speed digital system, Tx/Rx interface should be tested by S-parameter and Impedance.



◆ Transmitter Termination Effects (ADS simulation)



Transmitter Impedance **NOT** Matched



Transmitter Impedance Matched

PCIe 3.0 Tx/Rx Return Loss Test Solution

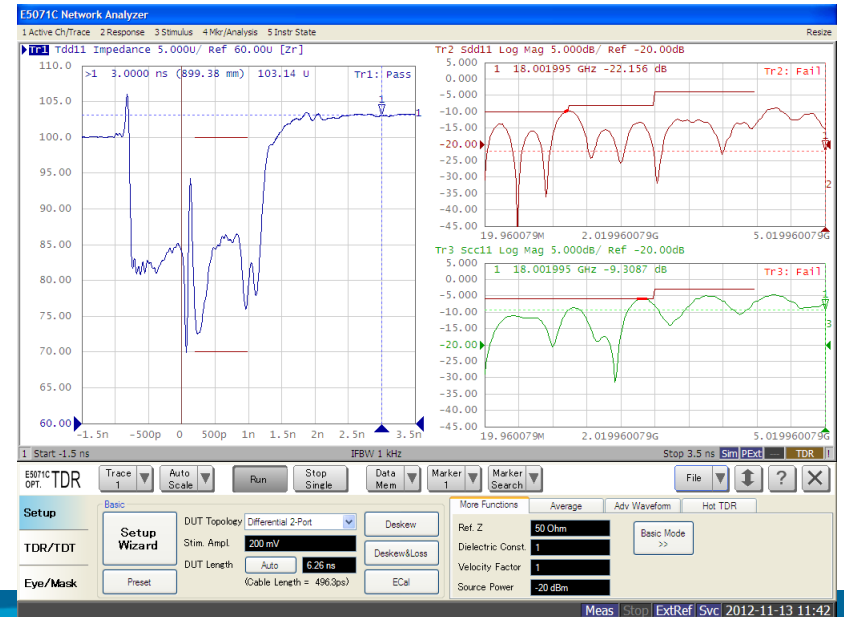
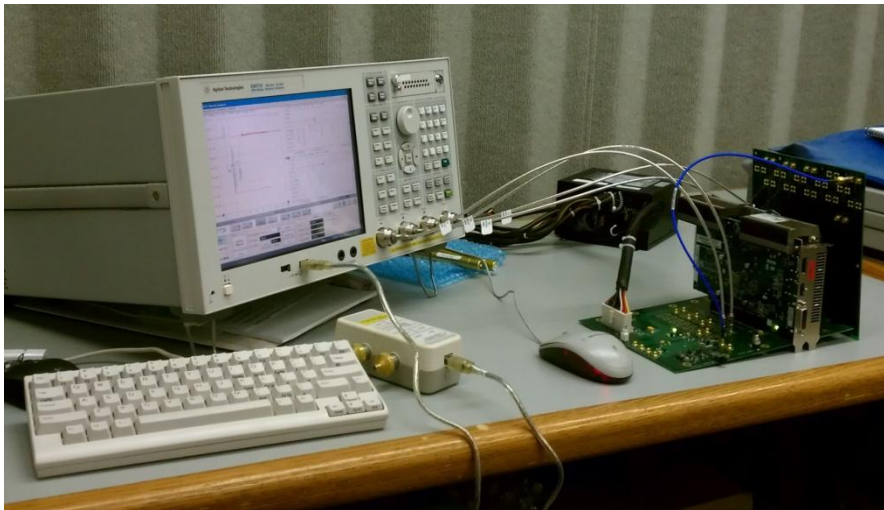
Measurement Parameters

◆Tx/Rx Return Loss Test (BASE Spec.)

	2.5 GT/s	5 GT/s	8 GT/s
Differential Return Loss	-10 dB	-8 dB	-4 dB @Tx / -5 dB @Rx
Common-mode Return Loss	-6 dB		-3 dB

The DUT must be powered up and DC isolated, and its data+/data- outputs must be in the low-Z state at a static value.

Measurement example of Add-in card return loss test:



PCIe 3.0 Tx/Rx Return Loss Test Solution

ENA Option TDR Solution



- ENA Mainframe
 - E5071C-480/480: 4-port, 9kHz/100kHz to 8.5GHz
 - E5071C-4D5: 4-port, 300kHz to 14GHz
 - E5071C-4K5: 4-port, 300kHz to 20GHz
- Enhanced Time Domain Analysis Option (E5071C-TDR)
- ECal Module
 - N4431B for E5071C-480/485
 - N4433A for E5071C-4D5/4K5

• Method of Implementation (MOI) document and state files will be available for download on Agilent.com

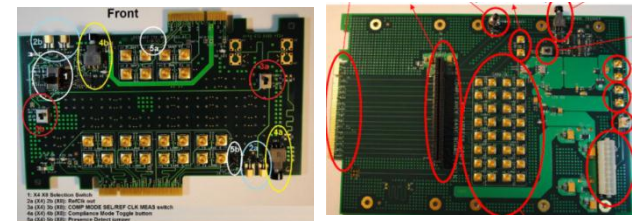
www.agilent.com/find/ena-tdr_compliance

PCI Express Test Fixtures

Specialized test fixtures available from the PCI-SIG:

- The **Compliance Load Board (CLB)** is used for testing platforms.
- The **Compliance Base Board (CBB)** is used for testing add-in cards.

The following links provide copies of the draft [CLB 3.0 Test Fixture User's Document](#) and the [CBB 3.0 Test Fixture User's Document](#). [Go to the CLB and CBB ordering instructions for more information.](#)

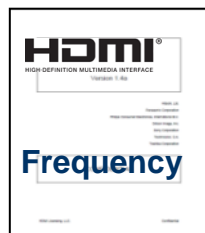
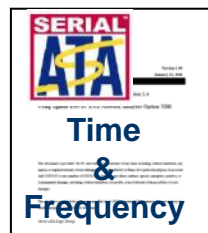
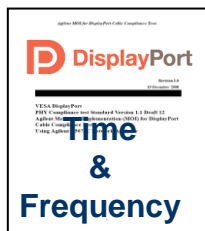


ENA Option TDR Compliance

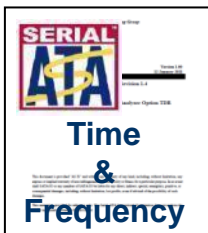
One-box Solution for TDR/S-parameter Compliance Test

Certified MOIs

•Cable/Connector



•Transmitter/Receiver (Hot TDR)



Test Centers Support ENA Option TDR

ENA Option TDR is used world wide by certified test centers of USB, HDMI, DisplayPort, and SATA



For more detail about compliance test solution by the ENA Option TDR, visit www.agilent.com/find/ena-tdr_compliance

PCIe 3.0 Test Solution

Summary



ENA Option TDR Cable/Connector Compliance Testing Solution is

- **One-box solution** which provides complete characterization of high speed digital interconnects (time domain, frequency domain, eye diagram)
- Similar look-and-feel to traditional TDR scopes, providing **simple and intuitive operation** even for users unfamiliar to VNAs and S-parameters
- Adopted by test labs worldwide



Questions?



PCI Express® Compliance Testing

<http://www.pcisig.com/specifications/pciexpress/compliance/>

The PCI-SIG provides PCI Express compliance tests that are utilized for testing PCI Express systems and add-in cards at each PCI-SIG [Compliance Workshop](#). The PCI-SIG also publishes an [Integrators List](#). For a PCI Express system, add-in card, or other device to be placed on the Integrators List, the system or device must pass interoperability and compliance testing, and the vendor must also submit a [Product Listing Request Form](#) for the system or device tested.

PCI Express Compliance Testing

There are five different test areas that make up PCI Express compliance testing.

- [Electrical testing](#): Examines platform and add-in card signal quality.
- [Configuration testing](#): Examines configuration space in PCI Express devices.
- [Link protocol testing](#): Tests device behavior for link-level protocol.
- [Transaction protocol testing](#): Tests device behavior for transaction level protocol.
- [Platform BIOS testing](#): Tests platform BIOS ability to recognize and configure PCI Express devices.

For a summary of the tests that are utilized at PCI-SIG Compliance Workshops for testing PCIe 2.0 and PCIe 3.0 products please see the [PCIe Workshop Testing Summary](#) (77kb pdf)

PCI Express® 3.0 Integrators List

http://www.pcisig.com/developers/compliance_program/integrators_list/pcie_3.0

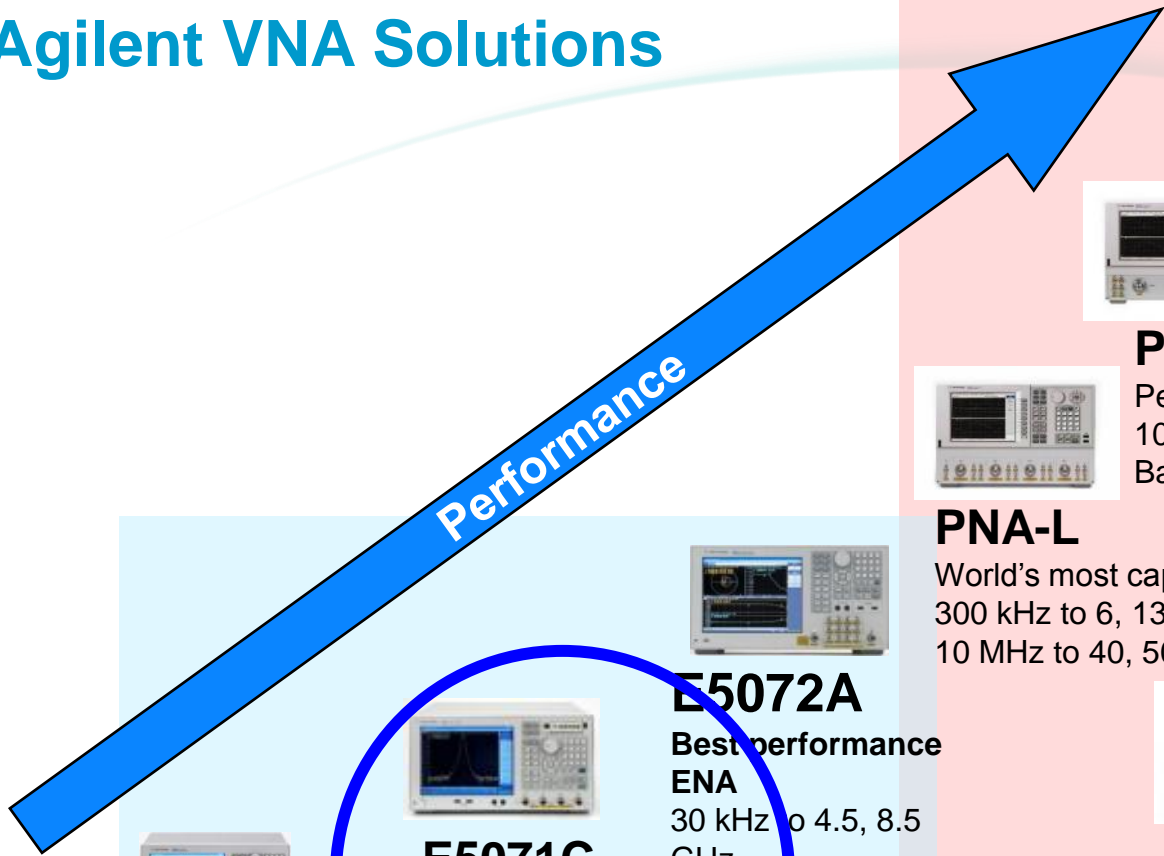
Another valuable benefit of the Compliance Program is inclusion on the PCI-SIG Integrators List. This list includes all products that have successfully completed the rigorous testing procedures of the Compliance Workshop. Inclusion on the list is only available to PCI-SIG member companies and cannot be used for individual marketing programs. However, many companies do refer to the list when making company-to-company purchases.

For a product to be listed on the Integrators List below, it must satisfy the following criteria:

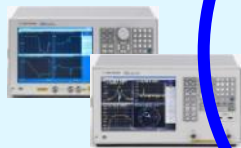
- Demonstrated interoperability (80% pass) at the Compliance Workshop.
- Demonstrated compliance to the applicable compliance test suite at the same Compliance Workshop.
- Completed [Product Listing Request Form](#) for the product tested, submitted to PCI-SIG following the Compliance Workshop. Submit forms to [PCI-SIG Tech Support](#).

This list will be updated after every Compliance Workshop.

Agilent VNA Solutions



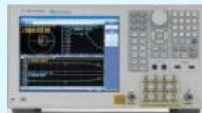
FieldFox
Handheld RF Analyzer
5 Hz to 4/6 GHz



E5061B
NA + ZA in one-box
5 Hz to 3 GHz
Low cost RF VNA
100 k to 1.5/3.0 GHz



E5071C
World's most popular economy VNA
9 kHz to 4.5, 8.5 GHz
300 kHz to 20.0 GHz



E5072A
Best performance ENA
30 kHz to 4.5, 8.5 GHz

ENA Series



PNA
Performance VNA
10 M to 20, 40, 50, 67, 110 GHz
Banded mm-wave to 2 THz



PNA-L
World's most capable value VNA
300 kHz to 6, 13.5, 20 GHz
10 MHz to 40, 50 GHz



PNA-X receiver
8530A replacement



Mm-wave solutions
Up to 2 THz



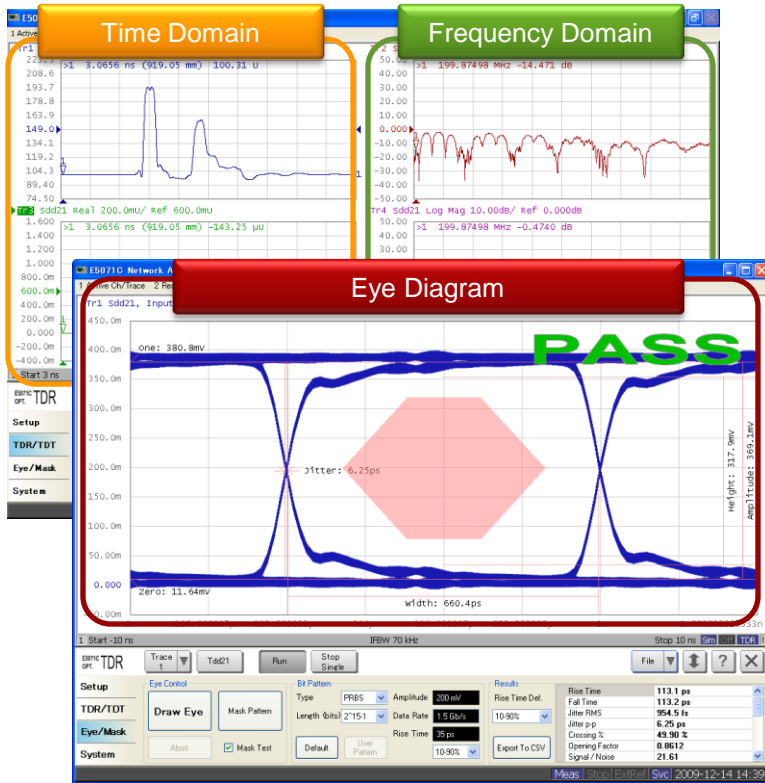
PNA-X, NVNA
Industry-leading performance
10 M to 13.5/26.5/43.5/50/67 GHz
Banded mm-wave to 2 THz

PNA Series

What is ENA Option TDR?

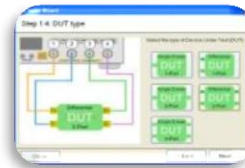


The ENA Option TDR is an application software embedded on the ENA, which provides an **one-box solution** for high speed serial interconnect analysis.



3 Breakthroughs

for Signal Integrity Design and Verification



Simple and Intuitive Operation



Fast and Accurate Measurements



ESD Robustness

What is ENA Option TDR?

[Video]

Agilent ENA Option TDR

Changing the world of Time Domain Reflectometry (TDR) Measurements

- www.youtube.com/watch?v=hwQNllyJ5hI&list=UUAJAJd97CfnCehC4jZAFkxQ&index=20&feature=plcp
- www.agilent.com/find/ena-tdr



Additional Resources



•ENA Option TDR Reference Material

www.agilent.com/find/ena-tdr

•Technical Overview (5990-5237EN)

•Application Notes

- Correlation between TDR oscilloscope and VNA generated time domain waveform (5990-5238EN)
- Comparison of Measurement Performance between Vector Network Analyzer and TDR Oscilloscope (5990-5446EN)
- Effective Hot TDR Measurements of Active Devices Using ENA Option TDR (5990-9676EN)
- Measurement Uncertainty of VNA Based TDR/TDT Measurement (5990-8406EN)
- Accuracy Verification of Agilent's ENA Option TDR Time Domain Measurement using a NIST Traceable Standard (5990-5728EN)

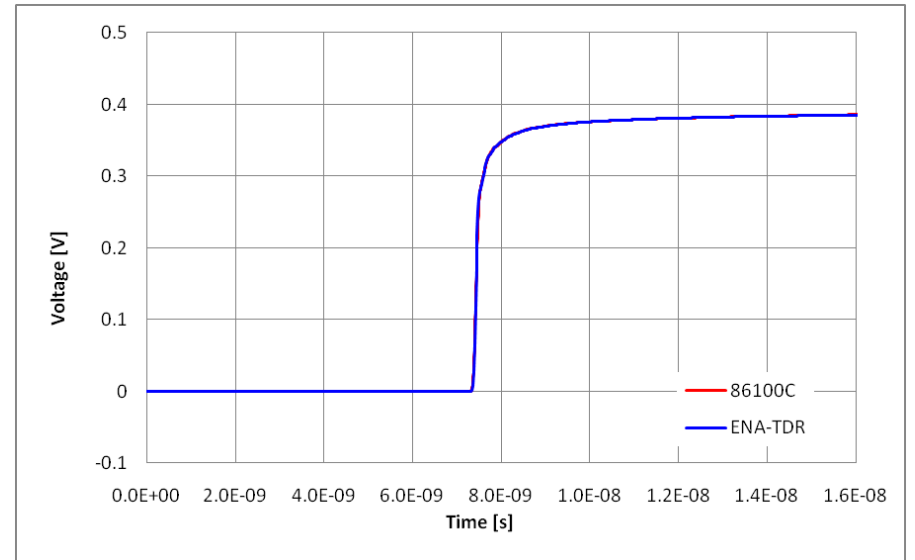
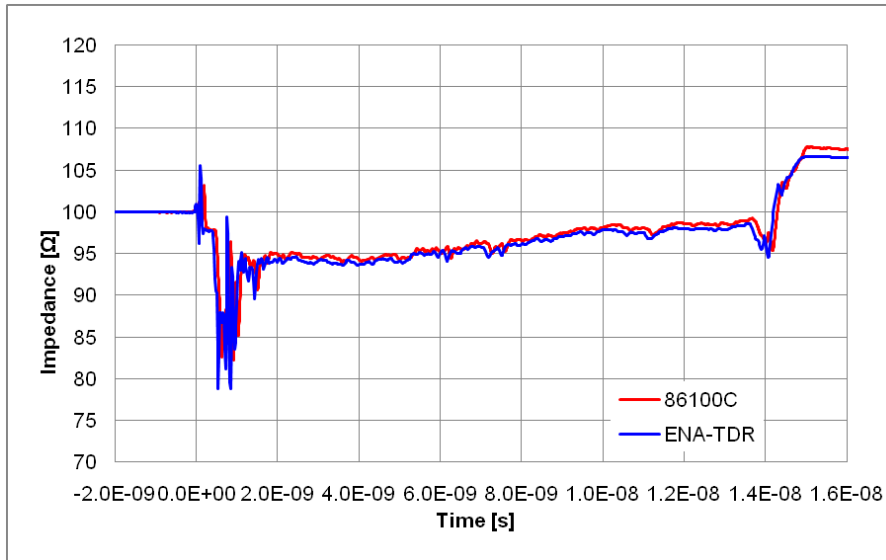
•Method of Implementation (MOI) for High Speed Digital Standards

www.agilent.com/find/ena-tdr_compliance

Measurement Correlation

TDR/TDT

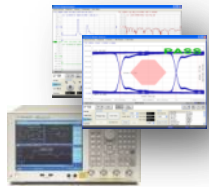
- DUT: USB3.0 Cable
- 50 ps rise time (20-80%)



Measurement Correlation

Eye Diagram

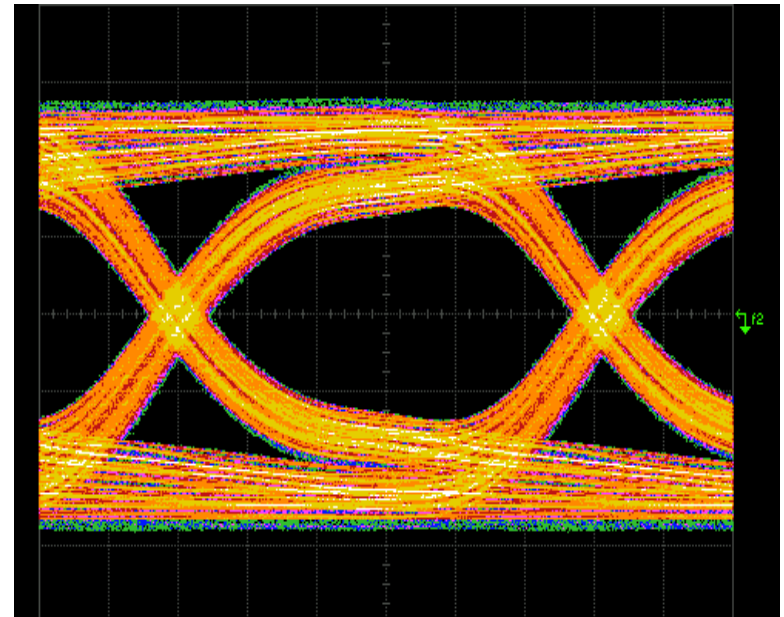
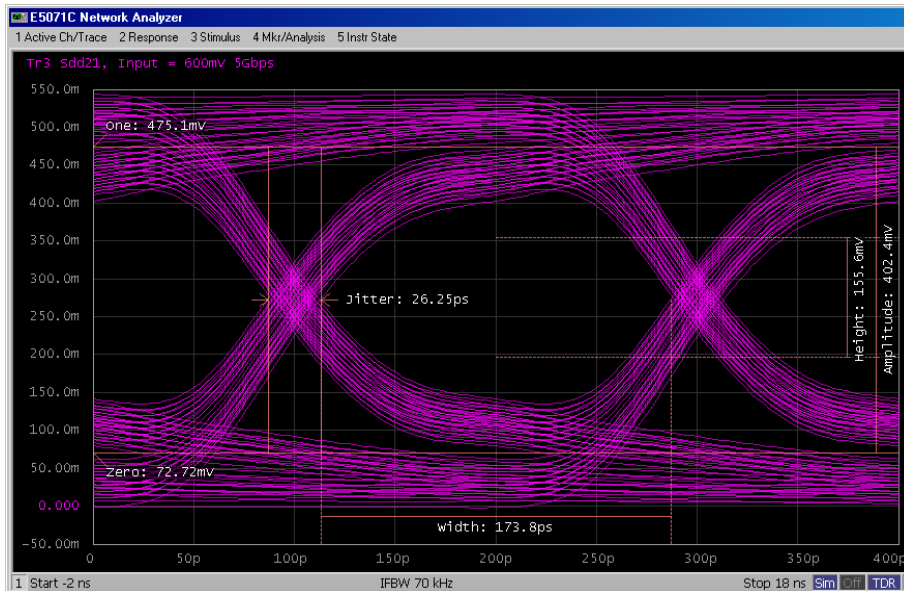
- DUT: USB3.0 Cable
- PRBS (2⁷-1) @ 5 Gbps



ENA Option TDR
(simulated)



N4903B + 86100C
(live)

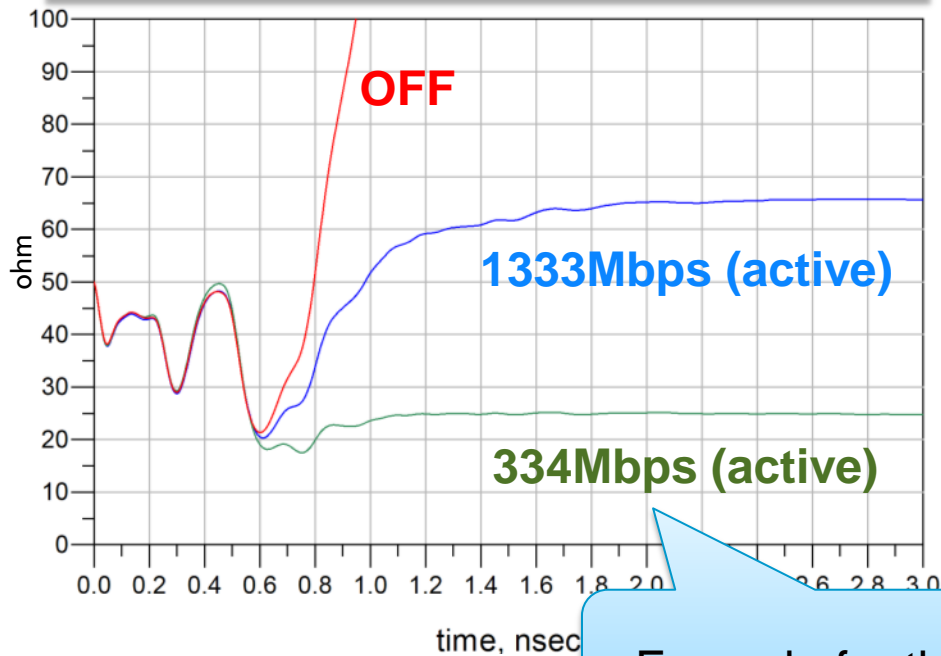


Hot TDR Measurements

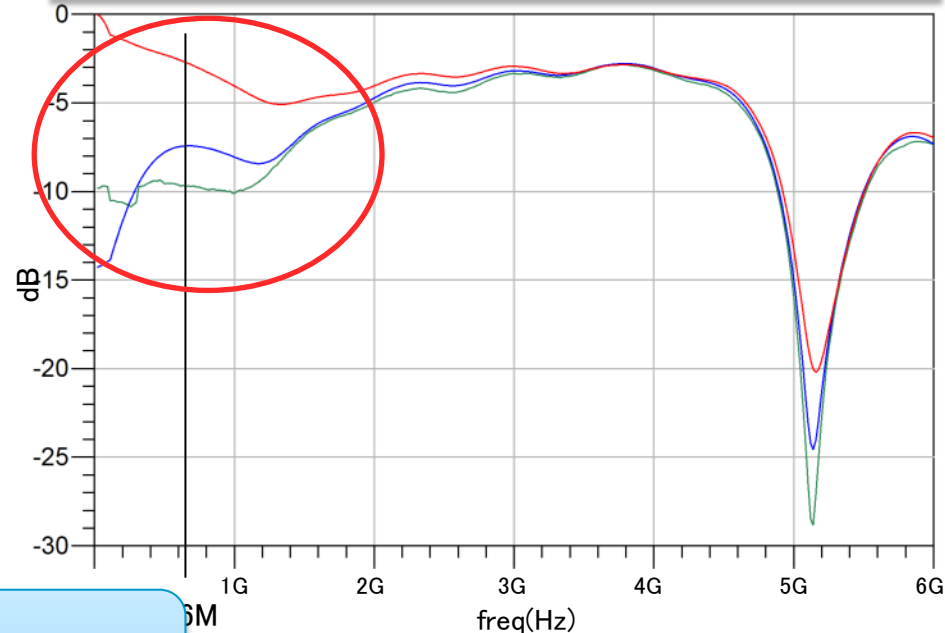
Why Measure?

- **Hot TDR** measurement is the impedance analysis of active devices under actual operation conditions.
- Typically, impedance of the device in the OFF state and ON state (Hot TDR) is significantly different. Impedance may vary with the data rate as well.

TDR (Time Domain)



Return Loss (Freq Domain)



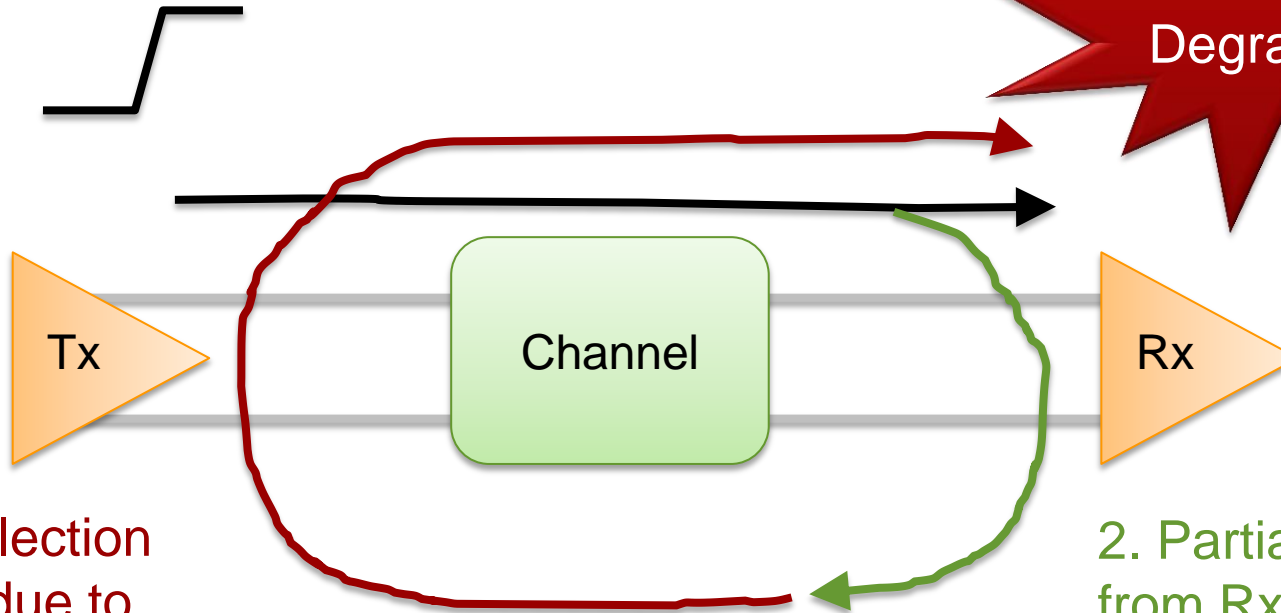
Example for the DDR

Hot TDR Measurements

Why Measure?

Multi-reflection effect to be more critical if bitrate increased.

1. Signal transmitted from Tx ...



Eye Degradation

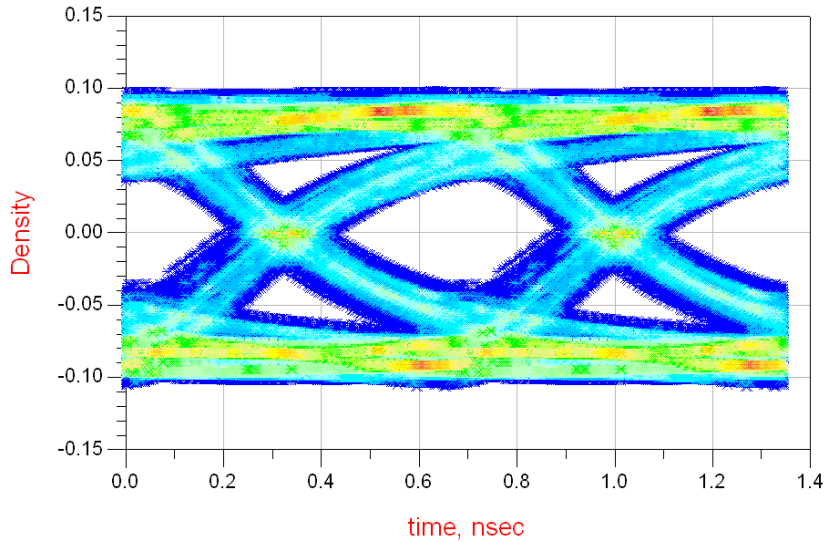
3. Re-reflection from Tx due to impedance mismatches ...

2. Partial reflection from Rx due to impedance mismatches ...

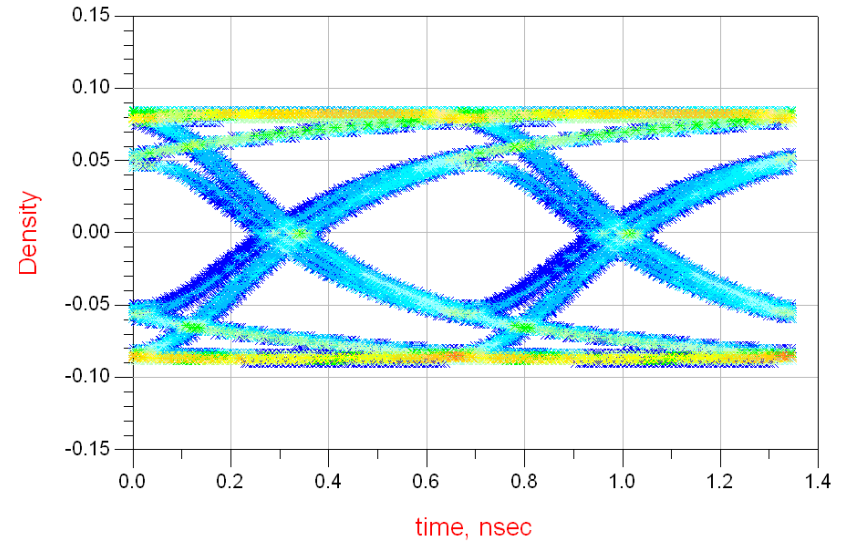
Hot TDR Measurements

Why Measure?

Source Termination Effects



Source Impedance **NOT** Matched

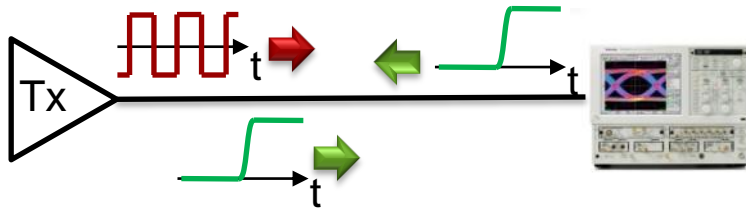


Source Impedance Matched

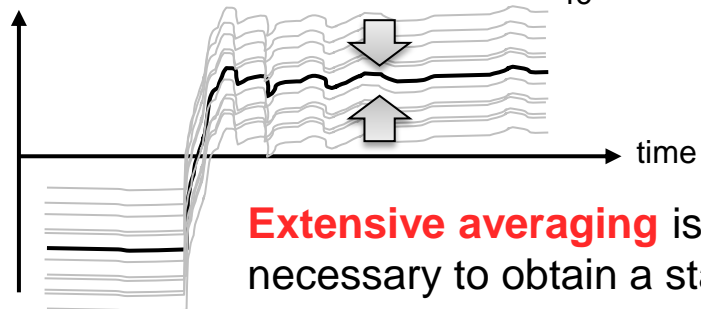
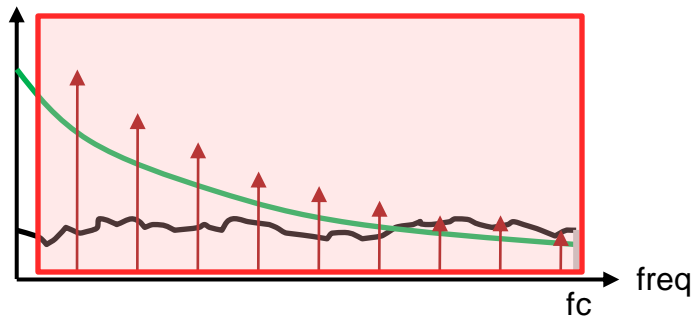
Advantages of ENA Option TDR for Hot TDR

Fast and Accurate Measurements

TDR Scopes

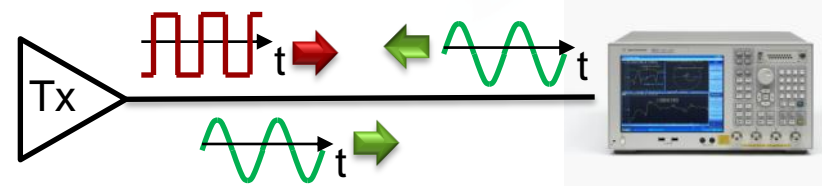


- **wideband receiver** captures all of the signal energy from the transmitter

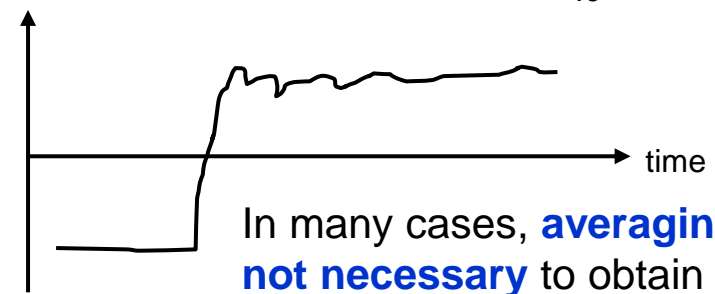
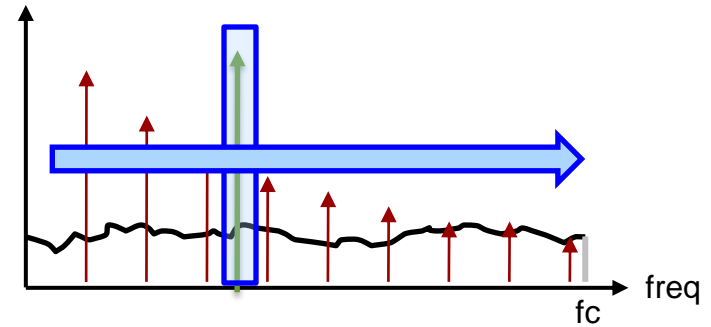


Extensive averaging is necessary to obtain a stable waveform.

ENA Option TDR



- **narrowband receiver** minimizes the effects of the data signal from the transmitter



In many cases, **averaging is not necessary** to obtain a stable waveform.

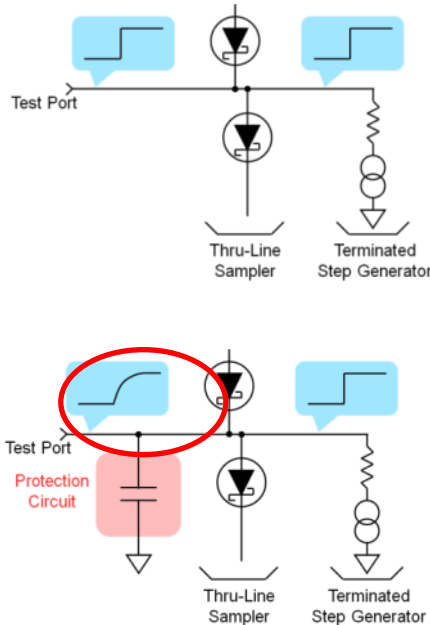
Advantages of ENA Option TDR for Hot TDR

ESD Robustness

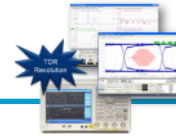
TDR Scopes



TDR scopes are sensitive to ESD.



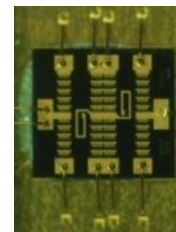
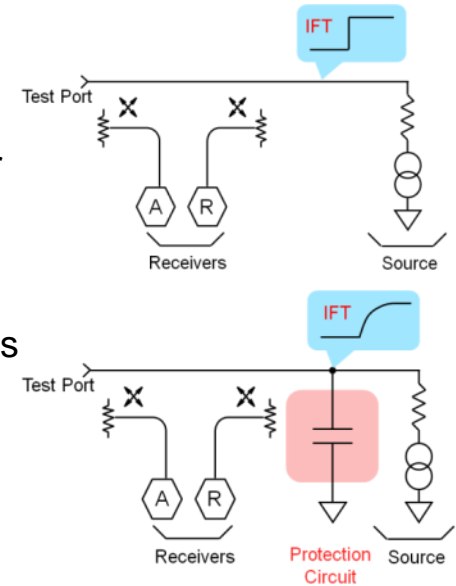
Implementing a protection circuit is difficult, because it will slow down the rise time of the step stimulus.



ENA Option TDR

ENA Option TDR has higher robustness against ESD, because protection circuits can be implemented more easily.

ENA Option TDR measures the vector ratios of the transmitted and received signals. Therefore, the effects of the protection circuit will be canceled out.



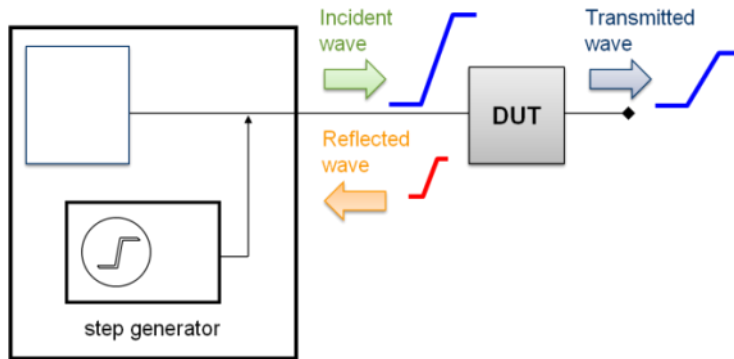
Proprietary ESD protection chip significantly increase ESD robustness, while at the same time maintaining **excellent RF performance** (22ps rise time for 20GHz models).



Advantages of ENA Option TDR for Hot TDR

Simple and Intuitive Operation

TDR Scopes



TDR scopes normally has a fixed TDR step voltage.

Attenuators are connected to the instrument to decrease amplitude to a level compliant with requirements.



ENA Option TDR

ENA Option TDR has internal variable attenuators, to allow for flexibility in setting the stimulus level to comply with requirements.

•Option 23x/24x/26x/28x/43x/44x/46x/48x

Range^{5, 6}

9 kHz to 5 GHz	-55 to 10 dBm
5 GHz to 6 GHz	-55 to 9 dBm
6 GHz to 7 GHz	-55 to 8 dBm
7 GHz to 8.5 GHz	-55 to 7 dBm

•Option 2D5/2K5/4D5/4K5

Range^{5, 6}

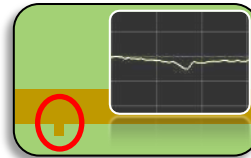
300 kHz to 1 MHz	-85 to 8 dBm
1 MHz to 6 GHz	-85 to 10 dBm
6 GHz to 8 GHz	-85 to 9 dBm
8 GHz to 10.5 GHz	-85 to 7 dBm
10.5 GHz to 15 GHz	-85 to 3 dBm
15 GHz to 20 GHz	-85 to 0 dBm

Advantages of ENA Option TDR for Hot TDR

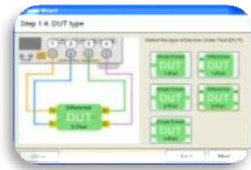
The **ENA Option TDR** is application software embedded on the ENA, which provides a **one-box solution** for high speed serial interconnect analysis.

3 Breakthroughs

for Hot TDR Measurements



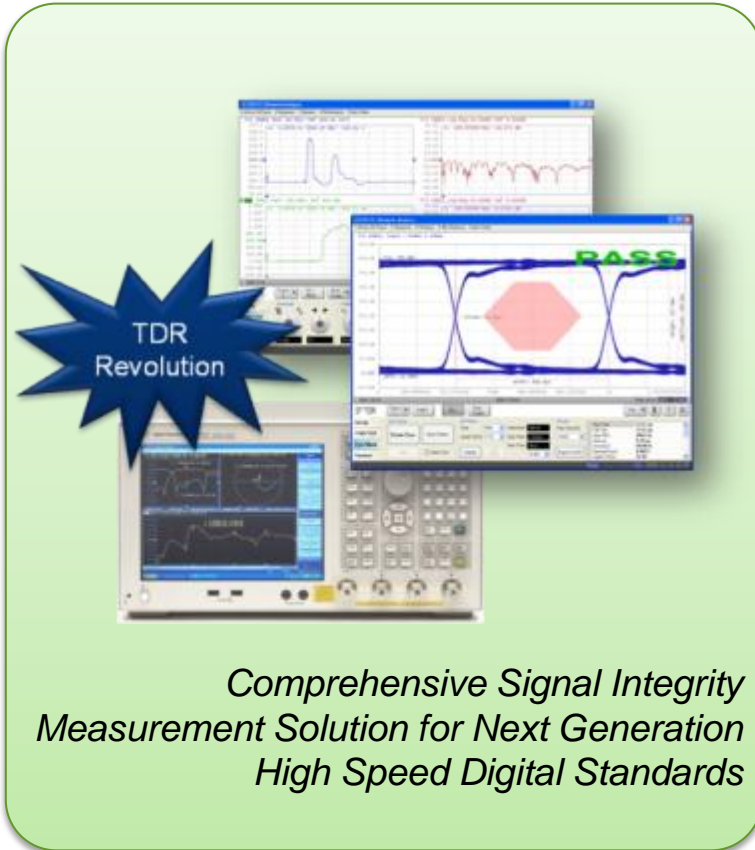
Fast and Accurate Measurements



Simple and Intuitive Operation



ESD Robustness



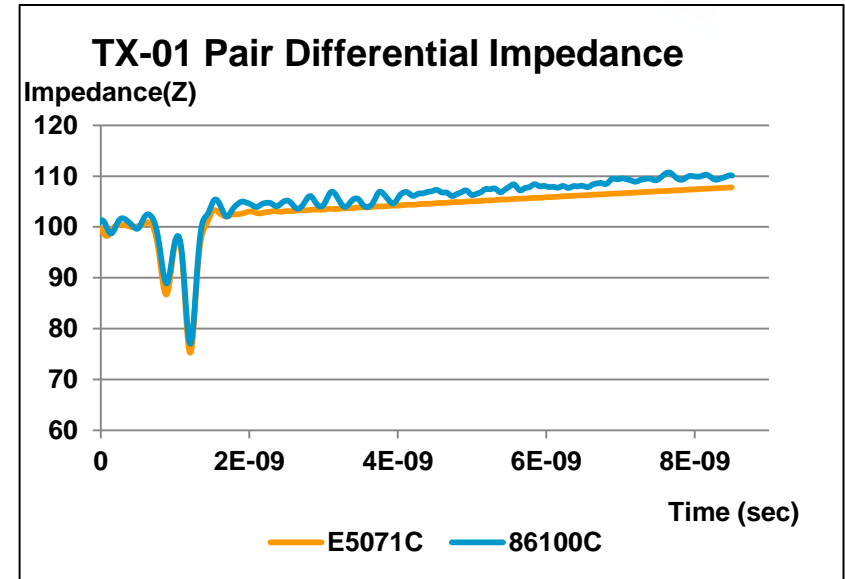
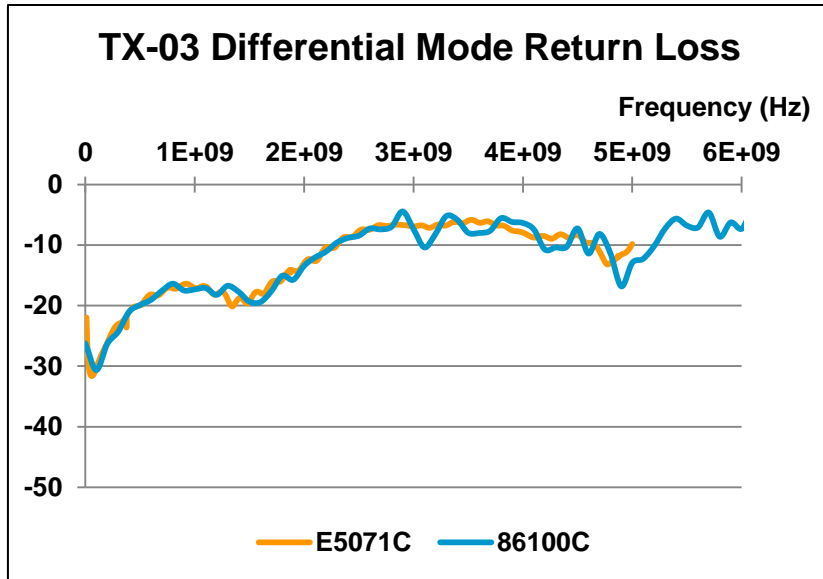
TDR Revolution

Comprehensive Signal Integrity Measurement Solution for Next Generation High Speed Digital Standards

Advantages of ENA Option TDR

Fast and Accurate Measurements

Correlation between 86100C TDR oscilloscope and E5071C ENA Option TDR



Time (sec)